



Children's Education Society
THE OXFORD COLLEGE OF ENGINEERING, BANGALORE - 560068
(Approved by AICTE, New Delhi, accredited by NBA, NAAC 'A'-Grade & Affiliated to VTU, Belagavi-590018)

B.E. Computer Science and Engineering
Outcome Based Education (OBE) and Choice Based Credit System (CBCS), VTU
ASSIGNMENT - II

Subject Code: BCS402

Semester / Section: IV/B

Subject Title: Microcontrollers

Submission Date: 29.05.2026

Course Objectives: Course Objectives:

CLO 1: Understand the fundamentals of ARM-based systems and basic architecture of CISC and RISC.

CLO 2: Familiarize with ARM programming modules along with registers, CPSR and Flags.

CLO 3: Develop ALP using various instructions to program the ARM controller.

CLO 4: Understand the Exceptions and Interrupt handling mechanism in Microcontrollers.

CLO 5: Discuss the ARM Firmware packages and Cache memory policies.

Q. NO	Questions	CO-PO
1	Discuss how ARM compilers can handle the basic C data types with an example.	CO3 - PO1,2,12
2	List and explain the most efficient ways to code for and while loops on the ARM processor.	CO3 - PO1,2,12
3	How the compiler attempts to allocate a processor register to each local variable used in C function?	CO3 - PO1,2,12
4	Define ARM Procedure Call Standard (APCS) and discuss ATPCS argument passing in C function.	CO3 - PO1,2,12
5	What is pointer aliasing and explain it with a simple example?	CO3 - PO1,2,12
6	Discuss how exception handling covers the specific details of how the ARM processor handles exceptions.	CO4 - PO1,2,12
7	Write the types of interrupts available on the ARM processor and discuss in detail.	CO4 - PO1,2,12
8	Define firmware and boot loader and write the stages of firmware execution flow in the ARM based system.	CO4 - PO1,2,12
9	What are the two industry standard firmware packages available for the ARM processor? Differentiate between ARM firmware suite and RED HAT REDBOOT.	CO4 - PO1,2,12
10	Discuss the directory layout of Sandstone and its execution flow.	CO4 - PO1,2,12
11	Draw the architecture of memory hierarchy and cache memory of a computer system and explain it.	CO5 - PO1,2,12
12	Draw a neat architecture of cache memory and explain its operations.	CO5 - PO1,2,12
13	List out the cache policies and discuss in detail.	CO5 - PO1,2,12
14	Simulate a program in C for ARM microcontroller using KEIL to sort the numbers in ascending/descending order using bubble sort.	CO5 - PO1,2,12
15	Simulate a program in C for ARM microcontroller to find factorial of a number.	CO5 - PO1,2,12

Course Outcomes:

CO1: Explain the ARM Architectural features and Instructions.

CO2: Develop programs using ARM instruction set for an ARM Microcontroller.

CO3: Explain C-Compiler Optimizations and portability issues in ARM Microcontroller.

CO4: Apply the concepts of Exceptions and Interrupt handling mechanisms in developing applications.

CO5: Demonstrate the role of Cache management and Firmware in Microcontrollers.

POs COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO3	1	2	-	-	-	-	-	-	-	-	-	1
CO4	1	2	-	-	-	-	-	-	-	-	-	1
CO5	2	1	-	-	-	-	-	-	-	-	-	2

a) Substantial(High)/3

b) Moderate(Medium)/2

c) Slight(Low)/1

d) No correlation/-

Faculty

HOD/CSE

Ms. J Jesy Janet Kumari

Deadline to submit the assignment is on or before 29th May 2026.